REMARKS

Claims 35-75 are pending in this application. By this Amendment, the drawings are replaced pursuant to the attached drawing sheets, claims 69 and 71 amended. Claim 69 is amended to recite features supported in the specification at page 8, line 17 – page 9, line 2 and Fig. 5. Claim 71 is amended to correct a minor informality. No new matter is added by any of these amendments.

Applicant appreciates the courtesies extended to Applicant's representative by Examiner Liang during the November 30, 2004 interview. In accordance with MPEP §713.04, the points discussed during the interview are incorporated in the remarks below and constitute Applicant's record of the interview.

Applicant gratefully acknowledges that claims 35-58 are allowed, and that claims 62, 64 and 72-75 contain allowable subject matter. However, Applicant asserts that all of claims 35-75 are allowable for the reasons discussed below.

Reconsideration based on the following remarks is respectfully requested.

I. Amendment Entry with Request for Continued Examination

Entry of this amendment is proper under 37 CFR §1.114 because this Submission is filed in conjunction with a Request for Continued Examination.

II. The Drawings are Corrected and Replaced with Formal Drawings

Fig. 7 was replaced in the November 9, 2004 Letter to the Official Draftsperson to correct T_{15} from representing a p-channel transistor to an n-channel transistor, as described at page 10, line 17. In the attached drawing sheets, Figs. 5 and 17 are replaced to remove the connecting dot between line V_2 and transistor T_B; Fig. 7 is replaced to correct T_7 from representing an n-channel transistor to a p-channel transistor, and to correct "V_{GO}" and "V_{SET}" to --V_{GP}-- and --V_{SEL}--, respectively; and Fig. 19 is replaced to correct T_7 from representing an n-channel transistor to a p-channel transistor, and T_{15} from representing a p-channel transistor to an n-channel transistor. Figs. 1 and 2 incorporate the changes provided

in the December 2, 2003 Amendment. Figs. 3, 4, 6, 8-16 and 18 as originally filed are also replaced with formal replacement sheets.

III. Claims 59-61, 63 and 65-71 Define Patentable Subject Matter

The Final Office Action rejects claims 69 and 70 under 35 U.S.C. §102(b) over U.S. Patent 5,714,968 to Ikeda. This rejection is respectfully traversed.

Ikeda does not teach or suggest a driving method to drive a driving circuit for a current driven element the driving method comprising setting at least one of a first operating voltage of a first transistor and a second operating voltage of a second transistor according to a data current at a level that corresponds to a data signal, and supplying a driving current to the current driven element through the first transistor and the second transistor, the data current flowing between a data line and a power source line, as recited in claim 69. This argument applies by extension to claim 70 based on its dependence from claim 69.

Instead, Ikeda discloses a light emitting drive circuit. In particular, Ikeda teaches controlling current through field-effect transistors 16, 17 by data lines 12, 13, switching transistors 14, 15 and capacitors 18, 19, with a constant current 3 provided at one of the transistor terminals (col. 8, lines 16-27, and Fig. 9 of Ikeda). Thus, Ikeda does not teach or suggest a data current flowing between a data line and a current line. Moreover, Ikeda uses a constant current 3, in contrast to the setting of operating voltages according to a data current, and thereby fails to anticipate Applicant's claimed features.

A claim must be literally disclosed for a proper rejection under §102. This requirement is satisfied "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference" (MPEP §2131). Applicant asserts that the Final Office Action fails to satisfy this requirement with Ikeda.

The Final Office Action further rejects claims 59-61, 63, 65-68 and 71 under 35 U.S.C. §103(a) over Ikeda. This rejection is respectfully traversed.

A *prima facie* case of obviousness for a §103 rejection requires satisfaction of three basic criteria: there must be some suggestion or motivation either in the references or knowledge generally available to modify the references or combine reference teachings, a reasonable expectation of success, and the references must teach or suggest all the claim limitations (MPEP §706.02(j)). Applicant asserts that the Final Office Action fails to satisfy these requirements with Ikeda.

In particular, Ikeda fails to teach or suggest driver circuit for driving a current driven element, the driver circuit comprising a first transistor, a second transistor, and a data current according to a data signal determining a first operating voltage of the first transistor and a second operating voltage of the second transistor, the first transistor being an n-channel transistor, the second transistor being a p-channel transistor, and a driving current that is supplied to the current driven element flowing through the first transistor and the second transistor, as recited in claim 59. These arguments apply by extension to claims 60-68 and 71 based on their dependence from claim 59.

Applicant's claimed features provide for the potentials and the conduction types of a transistor to determine which terminal of the transistor is the source and which is the drain. For example, an n-channel transistor has the source and drain correspond to terminals having the lower and higher potentials, respectively. Thus, as shown for example in Fig. 7, capacitor C_1 is connected between the terminal of the p-channel transistor T_{12} having the highest potential at the source and its gate. In addition, capacitor C_2 is connected between the terminal of the n-channel transistor T_{15} having the lowest potential at the source and its gate.

In contrast, Ikeda teaches in Fig. 9 that a current flows from the current source 3 to the common line 9. Thus, current flows in the same direction through both transistors 16, 17. Additionally, capacitor 18 is connected between common line 9 and the gate of transistor 16. Similarly, capacitor 19 is connected between common line 9 and the gate of transistor 17.

Hence, Ikeda teaches that the sources of both transistors 16, 17 must be disposed on the side of the common line 9, and thus must be of the same conduction type.

One of ordinary skill in the art would therefore recognize that if transistors 16, 17 of Ikeda were of alternate conduction types, the circuit configuration of Fig. 9 of Ikeda would not function. Consequently, the skilled artisan would interpret the portion of Ikeda cited in the Final Office Action (col. 9, lines 8-16 of Ikeda) to exclude the case where the two transistors have different conduction types from one another. Applicant's claims explicitly provide for separate operating voltages for n-channel and p-channel transistors determined by a data current. By requiring transistors to be on the same side of a line, Ikeda teaches away from Applicant's claimed features.

There is no motivation to modify features related to the fixed current through the transistors of Ikeda to provide that a data current, according to a data signal, determines first and second operating voltages of first and second transistors, respectively, as recited in Applicant's claims, nor has the Final Office Action established sufficient motivation for a *prima facie* case of obviousness. Even assuming that motivation to modify the applied reference is established, the modification fails to provide Applicant's claimed features.

For at least these reasons, Applicant respectfully asserts that the rejected independent claims are patentable over the applied references. The rejected dependent claims are likewise patentable over the applied references for at least the reasons discussed as well as for the additional features they recite.

Consequently, all the claims are in condition for allowance. Thus, Applicant respectfully requests that the rejections under 35 U.S.C. §§102 and 103 be withdrawn.

IV. Conclusion

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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Registration No. 27,075

Gerhard W. Thielman
Registration No. 43,186

JAO:GWT/gwt

Attachments:
Request for Continued Examination
Replacement Drawing Sheets (Figs. 1-19)

Date: January 28, 2005

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DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

Amendments to the Drawings:

The attached sheets of drawings include changes to Figs. 5, 7, 17 and 19, as discussed in the Remarks.

Additionally, the attached sheets of drawings include formal replacements for Figs. 1 and 2 as corrected in the December 2, 2003 Amendment, and Figs. 3, 4, 6, 8-16 and 18 as originally filed.

These sheets, which include Figs. 1-19, replace the original and previously replaced sheets including Figs. 1-19.

Attachment: Replacement Sheets: Figs. 1-19